

**SEMICONDUCTOR DEVICE**

Patent Number: JP64001269  
Publication date: 1989-01-05  
Inventor(s): WATANABE MASAYUKI; others: 04  
Applicant(s): HITACHI LTD; others: 03  
Requested Patent: ☒ JP64001269  
Application Number: JP19870155478 19870624  
Priority Number(s):  
IPC Classification: H01L25/04 ; H01L23/52 ; H01L25/08  
EC Classification:  
Equivalents: JP2603638B2

**Abstract**

**PURPOSE:** To improve the mounting density of a semiconductor chip on a module substrate by connecting the bump electrode of a semiconductor chip to leads, and connecting a plurality of the chips having leads to the wirings of the substrate.

**CONSTITUTION:** A module substrate 1 composed by a plurality of ceramic layers and wiring layers of laminated ceramics places 8 semiconductor chips 4A, 4B, 4C, 4D on its front and rear faces. It is not sealed with package made of ceramics or resin, and the face formed with semiconductor elements or wirings is molded with resin 7. Thus, the chips 4A, 4B, 4C, 4D connected with leads 5A, 5B, 5C, 5D by TABs to bump electrodes 6 are placed on the substrate 1 to construct a semiconductor device, thereby reducing the area of occupying the chips 4A, 4B, 4C, 4D on the substrate 1. Accordingly, the mounting density of the devices can be increased.

Data supplied from the esp@cenet database - 12